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A MICROCOMPUTER-BASED LOW-COST OMEGA NAVIGATION SYSTEM

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ABSTRACT

The application of a low-cost, commercially-available microcomputer as the navigation processor for a simplified OMEGA Navigation System (ONS) is an area of current research at Ohio University's Avionics Engineering Center. This paper describes the interface of a low-cost front-end OMEGA sensor to the microcomputer and gives an example of the phase-processing software and navigation routines being developed. Emphasis is placed on the description of results obtained with the software version of the OMEGA burst filter developed at Ohio University and known as the Memory-Aided Phase Locked Loop (MAPLL).

INTRODUCTION

In order to take advantage of the low-cost computing capability available with off-the-shelf microcomputers, a software-based ONS is being developed which minimizes hardware (and, therefore, size and cost). The design approach taken has been to utilize the ONS's previously developed front-end and a Kennedy incremental tape recorder to establish a data base of live OMEGA ground and flight data. This data base has been used as the input data in a FORTRAN language simulation analysis of the Ohio University ONS. The software phase processing routines developed have in turn been assembled in microcomputer code and implemented in the microcomputer.

A prototype OMEGA sensor processor previously developed at Ohio University and reported by Burhans[1] and Lilley[2] incorporated a hardware synchronization scheme, memory-aided digital phase lock loop (MAPLL), and LOP board. In order to utilize the microcomputer to its fullest capability and further reduce the cost of the ONS, it was desirable to implement these sensor processor functions in microcomputer software. An automatic synchronization technique has been simulated using the OMEGA data base, and it has been previously reported.[3]

A software phase lock loop with time constants and mode of operation closely resembling the hardware MAPLL has been simulated and lab-demonstrated on the microcomputer. The software MAPLL (SMAPLL) produces filtered phase estimates which have been used to plot LOP's which compare favorably with those produced by the hardware sensor processor. A description of the minimum-hardware ONS follows, and the paper concludes with an examination of the SMAPLL operation and its application to the very low-cost MINI-O system described by Burhans.[4]

RECEIVER-COMPUTER INTERFACE

The software-based ONS is illustrated functionally in Figure 1. The preamplifier and front-end modules have been described in detail by Burhans.[1] Raw OMEGA zero-crossings are provided by the front-end at a 10,200 Zps rate. The microcomputer interface module uses the irregularly-spaced OMEGA zero-crossings to sample a clock signal at some predetermined sample rate. An interrupt request signal is also generated at this sample rate and sent to the computer. This process has been previously described by Lilley and Salter.[3] The outputs of the interface module are, then, a digital word representing the phase of the current OMEGA zero-crossing with respect to a local clock and an interrupt request pulse which tells the computer that a new sample of OMEGA data is ready to be read.

Two versions of the interface module have been used at Ohio University. The first is a 100 Hz sampler designed to interface an airborne 30 Hz bandwidth front-end to the navigation processor for a general aviation aircraft. More recently, a 40 Hz sampling interface has been designed for the 4 Hz bandwidth MINI-O version which could see application as a low-cost educational tool or position-fixing aid for wilderness backpackers.

Although some currently available microcomputer systems include sophisticated input-output devices and interrupt servicing schemes, the very simple and inexpensive technique known as memory-mapped I/O is often adequate for the small-system dedicated application. This technique, as used in the interface module, is illustrated in Figure 2. When the computer recognizes the interrupt request, the first step in the interrupt service routine is to read the new phase data from location 8XXX. This memory address is hardware-decoded in the interface module as the location of the interface module's phase data latch. The decoding of this address enables a tri-state input switch which puts the data onto the computer's data bus. The data thus entered into the computer can then be manipulated by software routines to provide navigation information to the user (whether the user is a pilot, boat navigator, lab demonstrator, or backpacker).

COMPUTER-DISPLAY INTERFACE

As mentioned previously, memory mapping is an inexpensive, simple method for moving data into and out of the computer. Figure 3 shows the O.U. output circuitry which decodes a memory address to enable a latch. Note that this latch does not need to be a tri-state device since its inputs are enabled from the data bus only when enabled by the properly decoded address. It should also be pointed out that the address decoding circuitry is further simplified by decoding only the four most significant bits of the sixteen-bit address. (The particular microcomputer in use for the ONS development has a sixteen-bit address bus.) This in effect sacrifices 1K bytes of potential 64K memory locations (space which will probably never be needed by the dedicated small-system user). When the output latch address (e.g. 9XXX)is decoded, the latch is enabled to capture the current data bus bit pattern.

This can be current phase, miles-to-go, or any other data specified by the programmer. This digital word can then be converted to an analog voltage through a D/A resistor network and used to drive a chart recorder or meter (e.g. pilot's CDI or groundspeed meter).

SOFTWARE BURST FILTER

The microcomputer-based ONS is currently being used to demonstrate ONS routines as they are developed and refined in the FORTRAN simulation analysis. Using the OMEGA data base previously established, a routine has been developed to synchronize automatically the receiver-computer timing to the fixed OMEGA transmission pattern. This routine is documented in reference 3. After the ONS is in sync, the phase of each OMEGA transmitting station can be identified and tracked during each time slot or "burst" by a digital filter or phase locked loop.

An OMEGA burst filter concept developed at Ohio University and currently in use in the hardware OMEGA sensor processor, is the memory-aided phase locked loop (MAPLL).[5,6] Since the MAPLL has been shown to be an effective digital filter for estimating the phase of an OMEGA signal within a time slot, a software MAPLL (SMAPLL) with nearly the same loop characteristics was designed for the microcomputer-based ONS. The SMAPLL has been simulated in FORTRAN language, with the OMEGA data base serving as input data for the simulation. The SMAPLL has also been implemented in microcomputer code and used in the previously described microcomputer-based ONS to track live OMEGA phase. The hardware sensor processor's LOP board has been replaced with a simple software subtraction of two time slot phase outputs of the SMAPLL. This phase difference or LOP is then stored in the output latch previously described and (after D/A conversion) can be plotted on a chart recorder as shown in Figure 9.

To understand the operation of the SMAPLL it is helpful to review the characteristics of the hardware MAPLL. Figure 4 shows that the incoming OMEGA zero-crossings are compared to a locked reference pulse at a 10.2 KHz rate in a bilevel quantizing phase detector. If the incoming cycle of OMEGA is ahead of the locked phase the phase detector outputs a signal for the bi-directional loop counter to count up (and vice-versa). The loop counter is a sixteen bit up/down counter of which the six most significant bits are used as the locked reference phase. Therefore, it takes 1024 counts (correlated zero-crossings) in the same direction to increment or decrement the six-bit reference phase word. This amount of loop filtering was found to be optimum for the hardware MAPLL in terms of its ability to track low signal-to-noise ratio signals typical of the OMEGA environment.[6] The six-bit reference phase word is compared to a clock in a digital phase shifter which outputs the locked pulse, against which the incoming zero crossings are compared in the phase detector. At the end of each time slot, the locked reference phase word is stored in a random access memory until that time slot appears in the next ten second frame. It is then preloaded into the loop counter before measuring the new time slot phase.

The analogous block diagram for the SMAPLL operation appears in Figure 5. The operation of this software loop is similar to the MAPLL except that the hardware loop compares the position of an OMEGA zero-crossing with the locked pulse at a 10.2 KHz rate, while the software loop actually subtracts the incoming sampled phase word from the reference phase at some slower sampling rate (e.g. 100 Hz or 40 Hz). The software loop as initially implemented retains the MAPLL bilevel quantizing phase detector, operating at the 40 Hz interrupt rate. In order to operate the SMAPLL at speeds similar to the MAPLL, a 2-bit up/down counter precedes the six loop control bits. Future SMAPLL designs will draw on the inherent flexibility of software implementation and may contain a multi-level phase error quantization with appropriate weighting to obtain the narrowband performance of the MAPLL hardware loop.

MINI-O APPLICATION

The SMAPLL has been utilized as the burst filter for the low-cost MINI-O system. Operational and circuit details of the MINI-O system have been presented by Burhans.[7]

The MINI-O 4 Hz bandwidth front-end was configured with a microcomputer interface module which samples the OMEGA phase at a 40 Hz rate and provides the microcomputer with an interrupt request signal. Six-bit OMEGA phase data and two other timing-control signals are made available to the microcomputer at this 40 Hz sampling rate. Figure 7 shows the data format presented to the microcomputer. The software interrupt service routine then loads the data into the microcomputer using the memory-mapped input technique already described. The SMAPLL routine filters and tracks the phase measurements during each time slot as they arrive. The time slot phase estimates are then subtracted to form LOP's and the LOP digital word is output using the memory-mapped output latch. A flow chart of the SMAPLL routine used in the MINI-O system appears in Figure 6, and a listing of the micro-computer code used to implement the routine on an MCS6502-based JOLT system is given in Figure 8.

In order to compare the operation of the MAPLL and SMAPLL in the tracking of live OMEGA phase data, the hardware sensor processor (incorporating the hardware MAPLL) and the MINI-O SMAPLL LOP outputs were run side-by-side in the lab and their outputs plotted on a dual-trace chart recorder. An example of the resultant LOP charts appears in Figure 9.

NAVIGATION PROCESSOR ROUTINES

Since the sensor processor functions have been implemented in software, the next step is to develop an OMEGA tracking filter (with velocity-aiding) and efficient navigation processor routines for the microcomputer-based ONS. Conceptually, the OMEGA tracking filter takes the time slot phase estimates (once per time slot from the SMAPLL) and filters them over several time slots. It also incorporates velocity-aiding or second order characteristics to provide smoothed data to the navigation routine.

The navigation routine has as its inputs the position coordinates of the origin and destination, and current position as derived from OMEGA LOP's. It is the function of the navigation routine to produce a course deviation, miles-to-go to destination, and groundspeed information to the navigator.

SUMMARY

The Ohio University OMEGA hard , sensor processor functions, including automatic synchronization, phase locked loop burst filtering, and LOP generation, hr ,een simulated and the techniques developed are being implemented in microcomputer software. A description is provided f e software memory-aided phase locked loop (SMAPLL), and operational results have shown its operation to be similar to the hr .are MAPLL. A detailed description of the SMAPLL routine currently in use with the MINI-O receiver and JOLT microcomputo tem has been presented as an example of the potential for the development of a truly low-cost ONS. Development of navigat' oftware for the microcomputer-based ONS continues toward the goal of a completely software-based ONS costing less than $ 0.

ACKNOWI :DGEMENTS

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The authors gratefully acknowledge the contributions made by Ohio University's OMEGA project staff and students: Mr. Ralph W. Burhans, Project Engineer and inventor of the MINI-O system; Mr. Kent Chamberlin, Graduate Research Associate and developer of the MAPLL; Mr. Paul Blascho, Graduate Research Associate; and Mr. Lee Wright, Student Engineering Assistant.

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[1] Burhans, R. W., "Low-Cost, High-Performance VLF Receiver Front-End", Technical Memorandum (NASA) 18, Avionics Engineering Center, Ohio University, Athens, Ohio, September, 1975.

[2] Lilley, R. W., "Binary Processing and Display Concepts for Low-Cost Omega Receivers", Journal ION, Vol. 22, No. 3, Fall, 1975.

[3] Lilley, R. W., and R. J. Salter, "Simulation Analysis of a Microcomputer-Based Low-Cost Omega Navigation System", paper presented at National Aerospace Symposium of the ION, Warminster, Pennsylvania, April, 1976.

[4] Burhans, R. W., "The Mini-O, A Digital Superhet, or a Truly Low-Cost Omega Navigation Receiver", Technical Memorandum (NASA) 20, Avionics Engineering Center, Ohio University, Athens, Ohio, November, 1975.

[5] Chamberlin, K., "Binary Phase Locked Loops for Omega Receivers", Proceedings of the Second Omega Symposium, Washington, D.C., November, 1974.

[6] Chamberlin, K., "Digital Correlation Detector for Low-Cost Omega Navigation", Technical Memorandum (NASA) 19, CR144956, Avionics Engineering Center, Ohio University, Athens, Ohio, February, 1976.

[7] Burhans, R. W., "Mini-O, Simple Omega Receiver Hardware for User Education", paper presented at the International Omega Association First Annual Meeting, Arlington, Virginia, July, 1976.

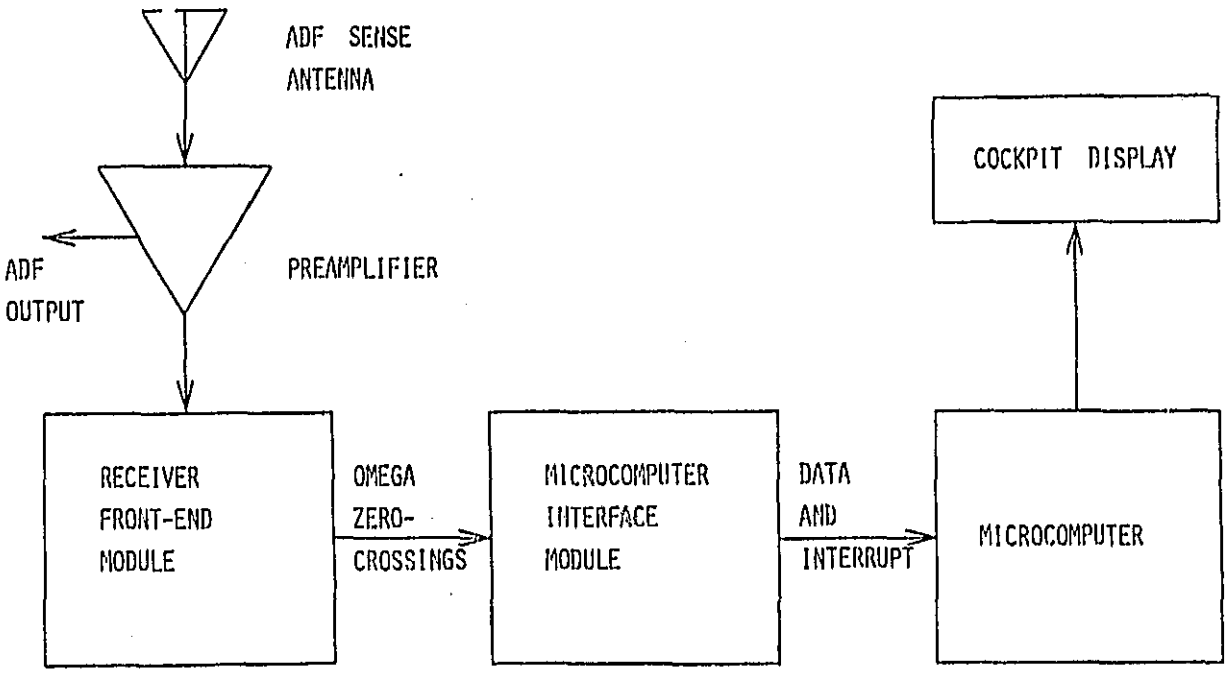

Figure 1. Summary Block Diagram - Microcomputer-Based OMEGA Receiver.

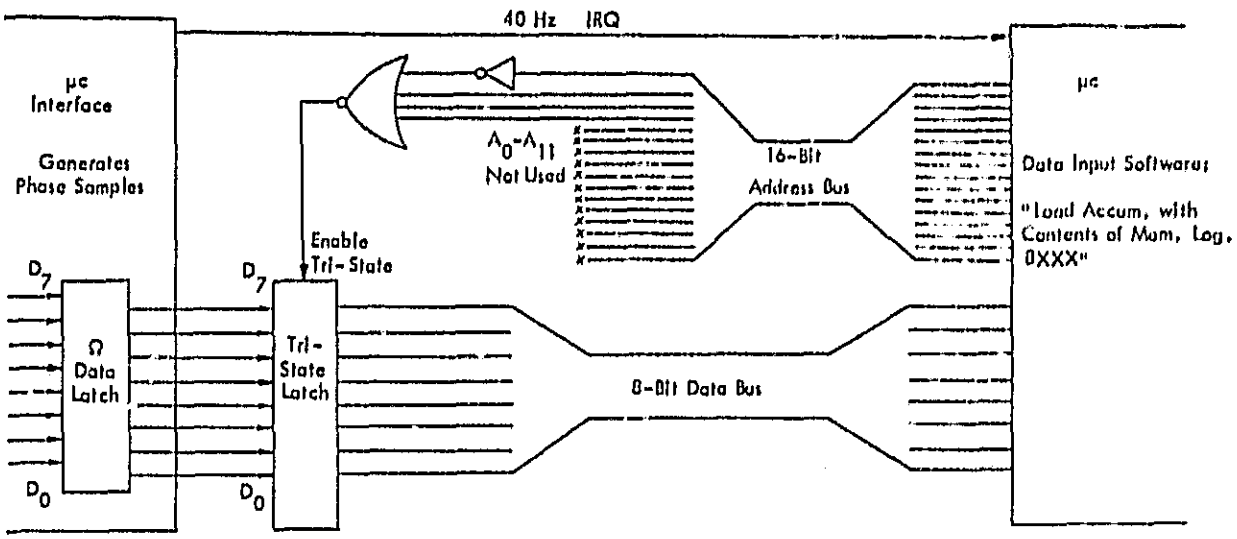

Figure 2. Microcomputer Input Interface.

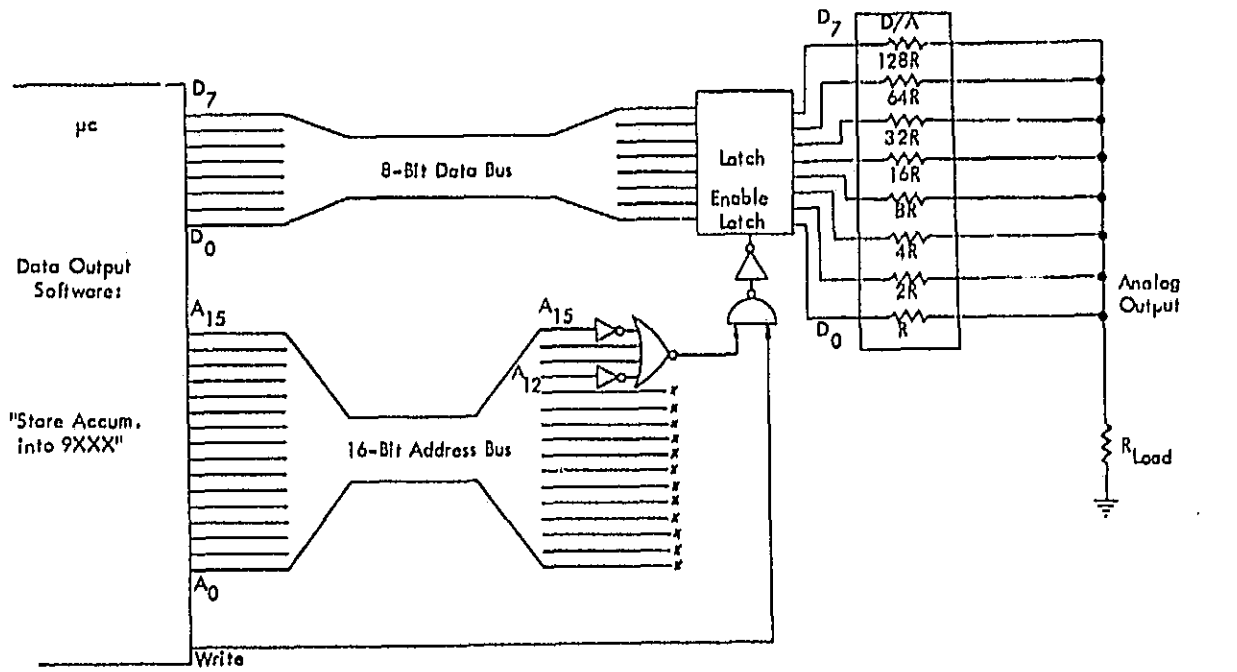

Figure 3. Microcomputer Output Interface.

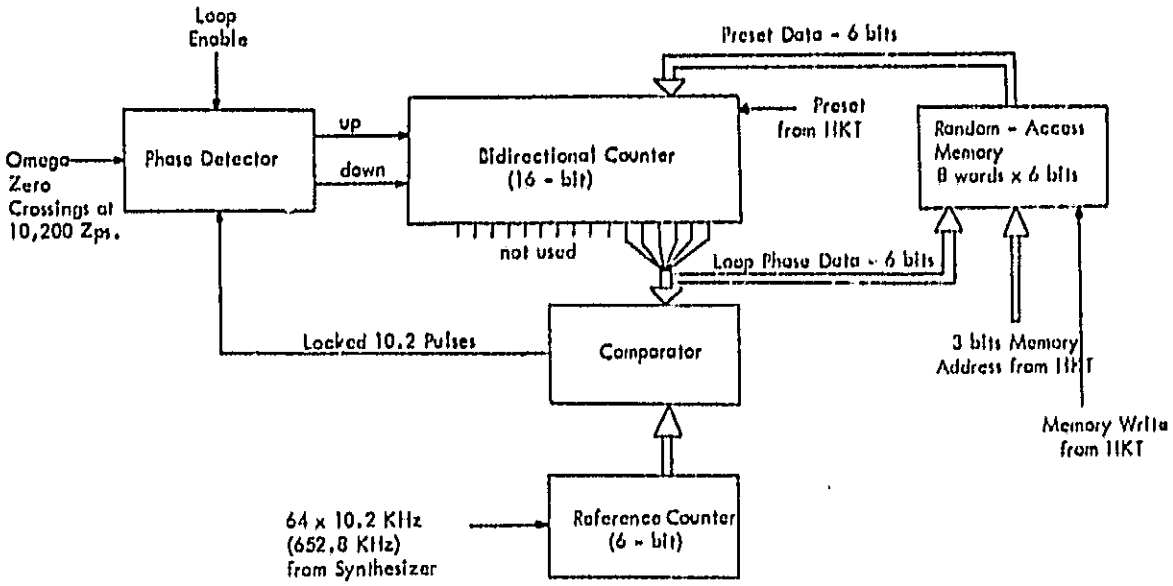

Figure 4. Memory-Aided Phase-Locked Loop (MAPLL).

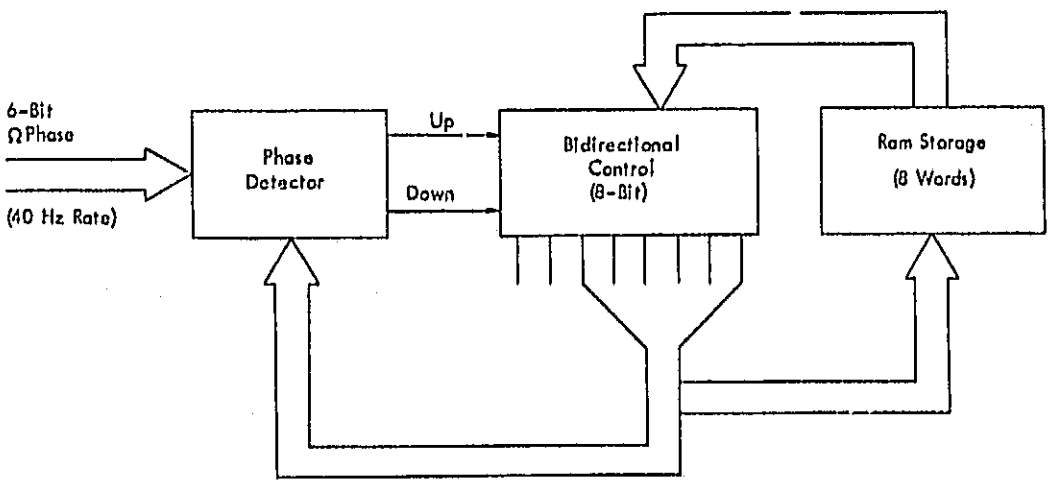

Figure 5. Software Memory-Aided Phase Locked Loop (SMAPLL).

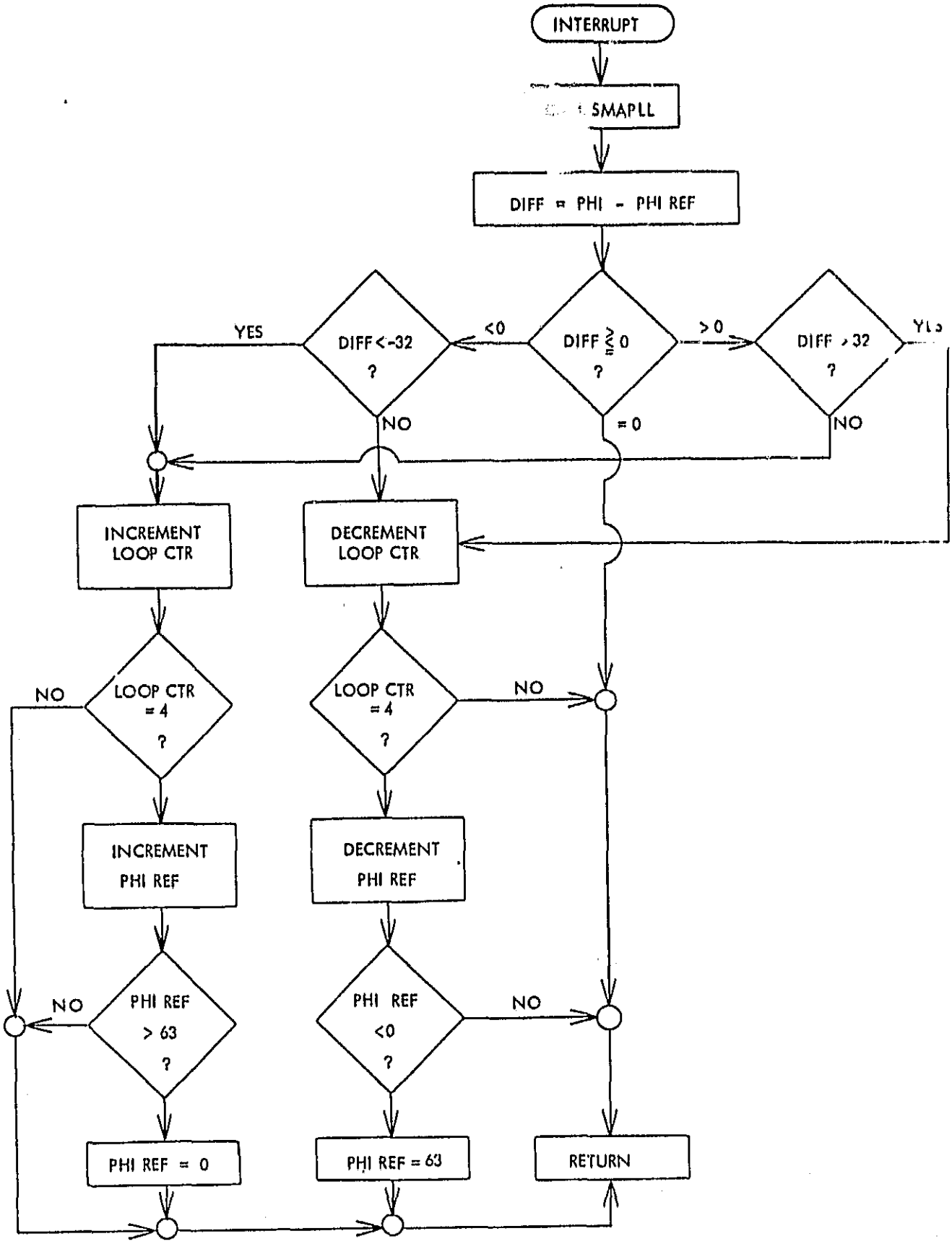

Figure 6. SMAPLL Flow Chart for 40 Hz Sampling, 6-Bit System.

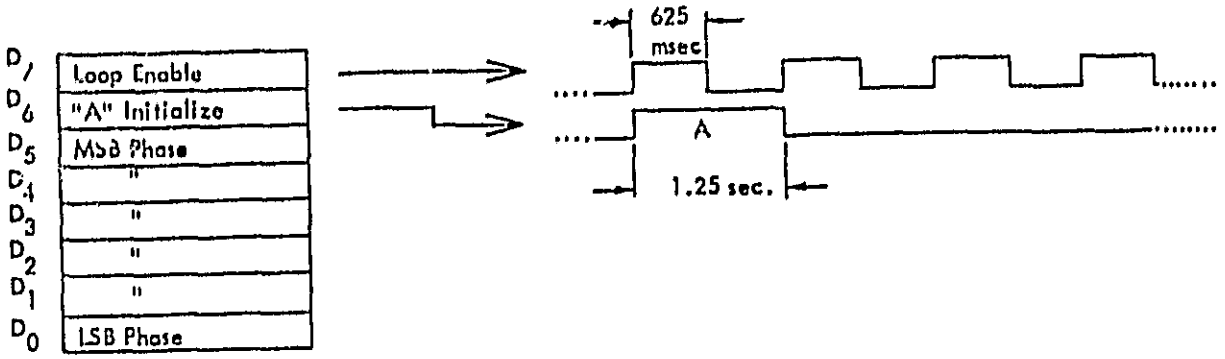

Figure 7. Mini-O Data Format.

```
.M  0000  AD 00 80 10 44 A2 80 86
.M  0008  E0 0A 10 04 A0 01 34 E1
.M  0010  4A 29 3F 35 D6 A6 E1 35
.M  0018  D7 4A 4A 35 D7 A5 D6 18
.M  0020  E5 D7 10 19 A5 D7 18 E5
.M  0028  D6 A3 A9 F6 85 3A A9 D6
.M  0030  85 37 93 C9 20 10 03 D6
.M  0038  D7 40 F6 D7 40 A3 A9 D6
.M  0040  85 3A A9 F6 35 37 4C 32
.M  0048  00 A5 E3 10 20 A0 00 34
.M  0050  E0 7C E0 04 F0 18 EA A5
.M  0058  D7 20 31 72 A5 E1 C9 03
.M  0060  D0 06 20 8A 72 4C 63 00
.M  0068  20 77 73 E6 E1 40 A5 DA
.M  0070  4A 4A 35 D3 A5 D7 18 E5
.M  0078  D3 30 03 3A 0A 3D 00 90
.M  0080  4C 57 00 60 40 4C 73 00
.M  0088  4C 00 00 91 1C E5 18 90
.
```

Beginning Memory Location (HEX)

Microcomputer Code

Figure 8. JOLT System Listing for MINI-O SMAPLL.

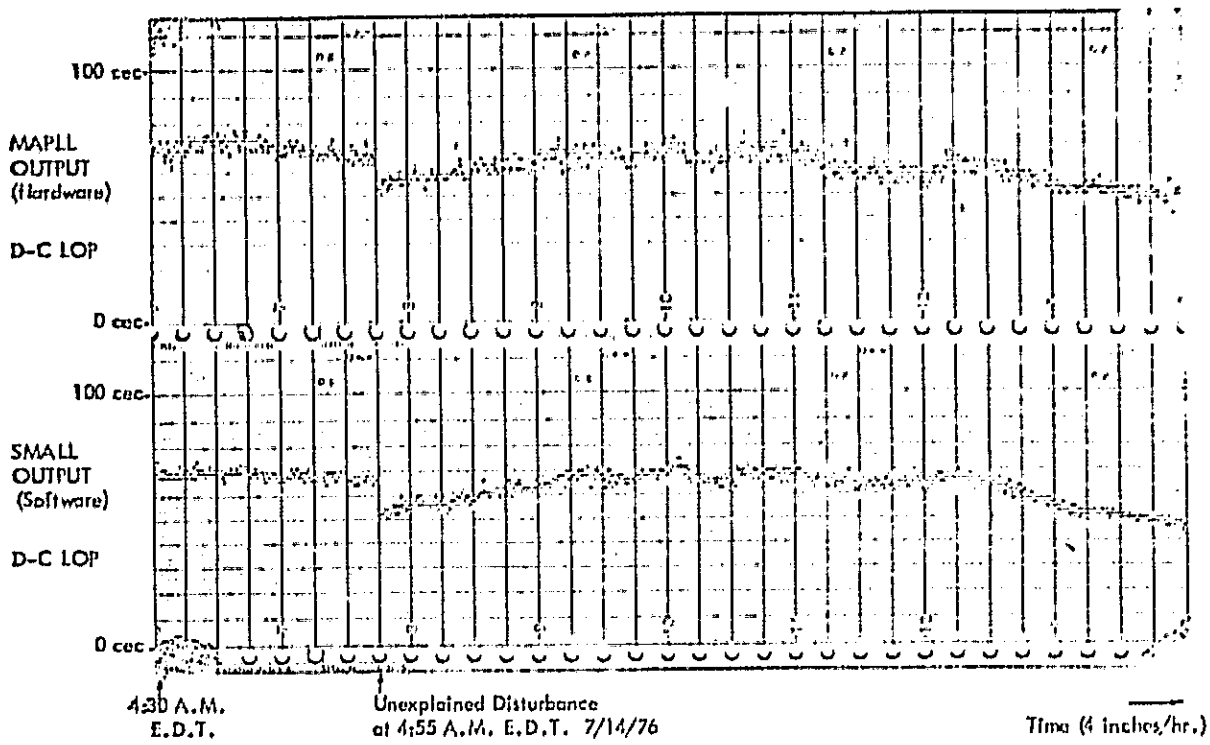

Figure 9. OMEGA LOP Traces -- Software Loop Output on Bottom.

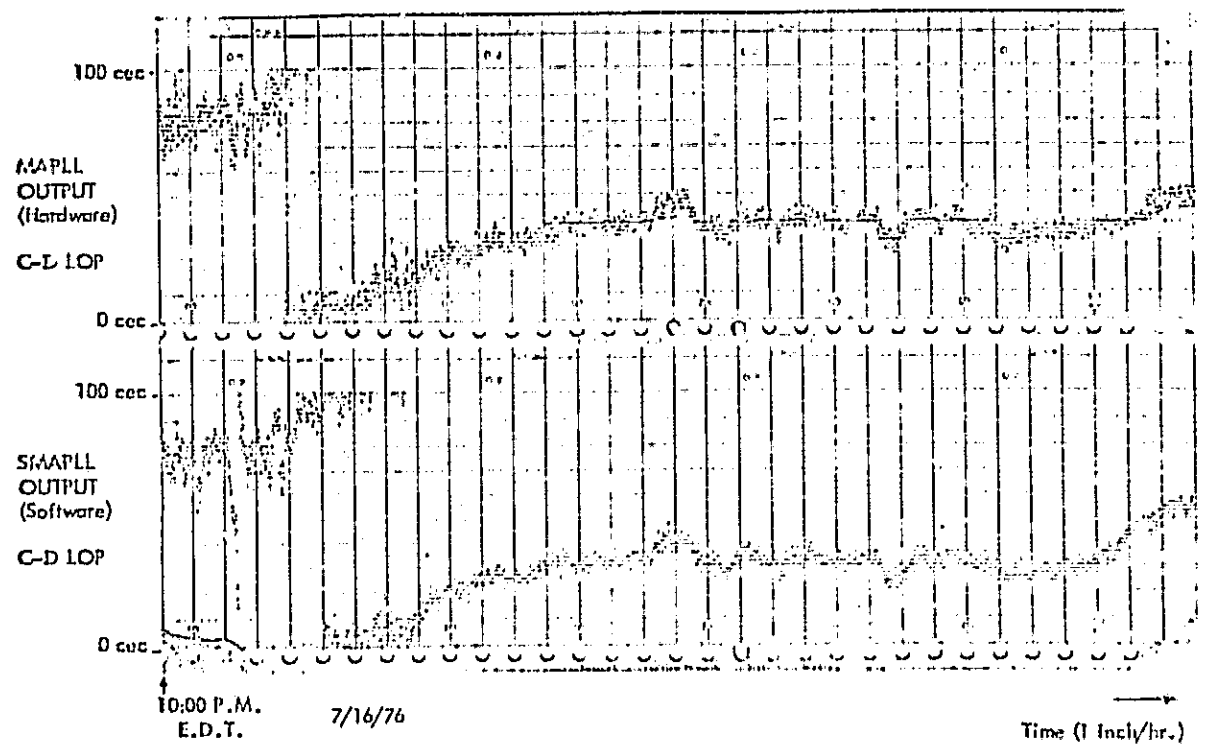

Figure 10. OMEGA LOP Output Traces -- Software Loop Output on Bottom.